**COMP 2601**

**Tutorial 7**

**Question 1**

A computer has 1Mbyte of RAM, word size of 1 byte, block size of 16 bytes and a cache size of 64 Kbytes. Determine how a memory address CABBF is interpreted if the cache is a:

1. Direct-mapped cache [5 marks]
2. Fully- associative cache [3 marks]
3. Two-way set associative cache. [4 marks]

**Question 2**

Consider a two-way set associative cache with a line size of 8 bytes. The cache can accommodate a total of 8 Kbytes. The main memory size that is cacheable is 256 Kbytes and word size is 1 byte. Determine the number of sets in the cache, size of a memory address and the size of the tag, set and word fields. [6 marks]

**Question 3**

A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

**Question 4**

A two-way set-associative cache has lines of 16 bytes and a total size of 8 kB. The 64-MB main memory is byte addressable. Show the format of main memory addresses.

**Question 5**

Consider a 32-bit microprocessor that has an on-chip 6-kB four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache is the word from memory location ABCDE8F8 mapped?

**Question 6**

Differentiate between direct mapping and set-associative mapping.